

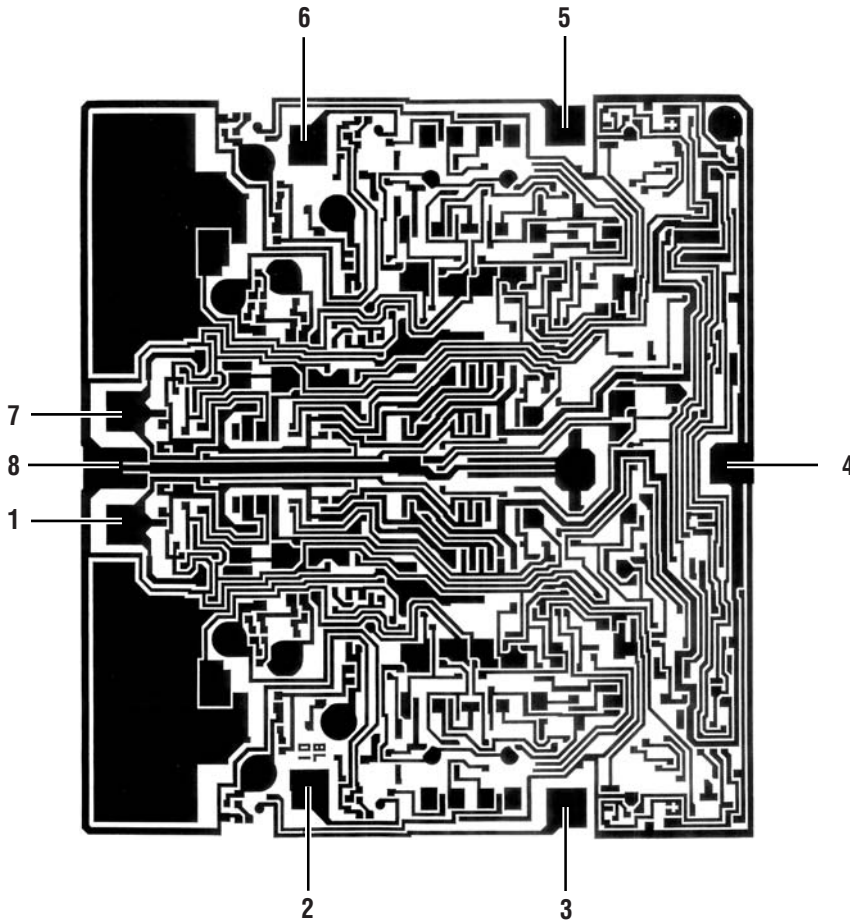
DIE CROSS REFERENCE

LTC Finished Part Number	Order DICE CANDIDATE Part Number Below
RH1078M	RH1078M DICE

PAD FUNCTION

1. OUTA
2. -INA
3. +INA
4. -V
5. +INB
6. -INB
7. OUTB
8. +V

12mils thick,
backside (substrate) is an alloyed
gold layer. Connect backside to V^- .



90 × 97 mils

DICE ELECTRICAL TEST LIMITS

$V_S = 5V$, $V_{CM} = 0.1V$, $V_{OUT} = 1.4V$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	$T_A = 25^\circ C$		UNITS
			MIN	MAX	
V_{OS}	Input Offset Voltage			120	μV
I_{OS}	Input Offset Current			0.8	nA
I_B	Input Bias Current			15	nA

DICE SPECIFICATION

RH1078M

DICE ELECTRICAL TEST LIMITS $V_S = 5V$, $V_{CM} = 0.1V$, $V_{OUT} = 1.4V$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	$T_A = 25^\circ C$		UNITS
			MIN	MAX	
CMRR	Common Mode Rejection Ratio	$V_{CM} = 0V$ to $3.5V$ $V_{CM} = 0.05V$ to $3.2V$	94		dB dB
PSRR	Power Supply Rejection Ratio	$V_S = 2.3V$ to $12V$ $V_S = 3.1V$ to $12V$	100		dB dB
A_{VOL}	Large-Signal Voltage Gain	$V_O = 0.03V$ to $4V$, No Load $V_O = 0.03V$ to $3.5V$, $R_L = 50k$ $V_O = 0.05V$ to $4V$, No Load $V_O = 0.05V$ to $3.5V$, $R_L = 50k$	150 120		V/mV V/mV V/mV V/mV
V_{OUT}	Output Voltage Swing	Output Low, No Load Output Low, $2k$ to GND Output Low, $I_{SINK} = 100\mu A$ Output High, No Load Output High, $2k$ to GND	4.2 3.5	6 2 130	mV mV mV V V
SR	Slew Rate	$A_V = 1$, $V_S = \pm 2.5V$	0.04		V/ μs
I_S	Supply Current	Per Amplifier		75	μA
	Minimum Supply Voltage	Note 1		2.3	V
V_{OS}	Input Offset Voltage			350	μV
I_{OS}	Input Offset Current			0.8	nA
I_B	Input Bias Current			15	nA
	Input Voltage Range		13.5 -15.0		V V
CMRR	Common Mode Rejection Ratio	$V_{CM} = 13.5V$, $-15V$ $V_{CM} = 13V$, $-14.9V$	97		dB dB
PSRR	Power Supply Rejection Ratio	$V_S = 5V$, $0V$ to $\pm 18V$	100		dB
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 50k$ $V_O = \pm 10V$, $R_L = 2k$ $V_O = \pm 10V$, $R_L = 5k$	1000 300		V/mV V/mV V/mV
V_{OUT}	Output Voltage Swing	$R_L = 50k$ $R_L = 2k$ $R_L = 5k$	± 13 ± 11		V V V
SR	Slew Rate		0.06		V/ μs
I_S	Supply Current	Per Amplifier		100	μA

Note 1: Power supply rejection ratio is measured at the minimum supply voltage.

Wafer level testing is performed per the indicated specifications for dice. Considerable differences in performance can often be observed for dice versus packaged units due to the influences of packaging and assembly on certain devices and/or parameters. Please consult factory for more information on dice performance and lot qualifications via lot sampling test procedures.

Dice data sheet subject to change. Please consult factory for current revision in production.

I.D.No. 66-13-1078